

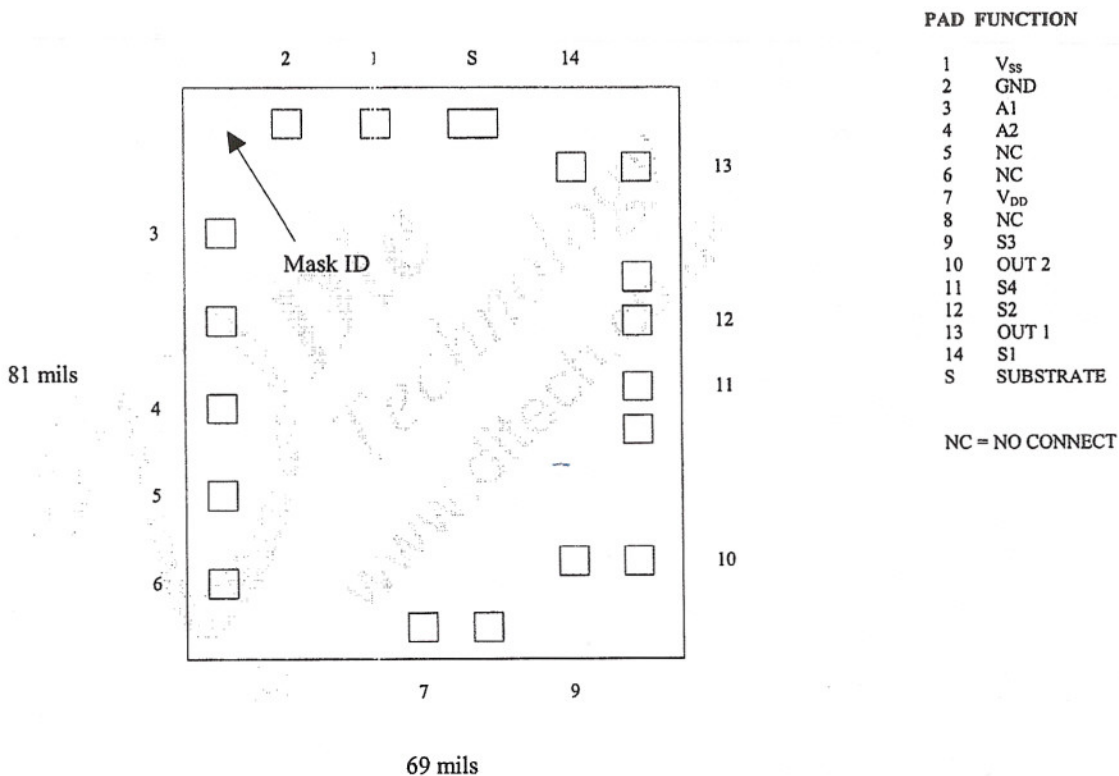


# Sierra Components, Inc.

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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



NOTE: Substrate must be connected to V<sub>DD</sub>

**Topside Metal: Aluminum**  
**Backside Metal: Silicon**  
**Backside Potential: V<sub>DD</sub> (See Note)**  
**Bond Pad Size: .004" Min.**  
**Mask Ref: B03**

MFG: Analog Devices

THICKNESS: .020"

Part # AD7512

APPROVED BY: R Bacon

DIE SIZE : .069"x .081"

DATE: 11/2/09